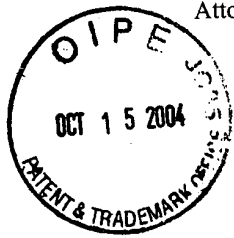


Application No.: 10/043,946  
Attorney Docket: AMKOR-017RCE



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants: Jong Sik Paek ) Confirmation No. 2822  
Serial No.: 10/043,946 ) Art Unit: 6383  
Filed: 01/11/2002 ) Examiner: Lewis,  
For: SEMICONDUCTOR PACKAGE ) Monica  
WITH STACKED DIES )

**APPEAL BRIEF UNDER 37 C.F.R. § 1.192**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir/Madam:

Applicant [hereinafter "Appellant"], in the above-captioned patent application, has appealed from the Examiner's final rejection of Claims 1-9, 11 and 19-24 as set forth in the Final Office Action of May 19, 2004.

A Notice of Appeal in response to the Final Office Action was filed on September 17, 2004. The Appeal Brief is being submitted in triplicate pursuant to 37 C.F.R. § 1.192(a) with the requisite fee under 37 C.F.R. § 1.17(c) in the amount of \$330. An ORAL HEARING IS NOT REQUESTED.

If for any reason the necessary fee is not associated with this file, the Commissioner is authorized to charge the appropriate fee for the Appeal Brief and/or any necessary extension of time fees to Deposit Account Number 19-4330.

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**I. REAL PARTY IN INTEREST**

The real party in interest is Amkor Technology, Inc. by assignment recorded in the U.S. Patent and Trademark Office on January 11, 2002 at Reel 012478, Frame 0410.

**II. RELATED APPEALS AND INTERFERENCES**

No related appeals and/or interferences are pending.

**III. STATUS OF CLAIMS**

Claims 1-9, 11 and 19-24, the only claims pending in the subject application, stand finally rejected (see Appendix entitled "CLAIMS ON APPEAL").

**IV. STATUS OF AMENDMENTS AFTER FINAL**

There are no un-entered amendments.

**V. SUMMARY OF INVENTION**

There has been developed in the prior art various semiconductor packages in which the internal semiconductor dies of the package or the semiconductor packages themselves are stacked on each other. For instance, Figure 7 of U.S. Patent No. 6,198,171 to Huang et al. teaches a semiconductor package 302a having stacked chips 304, 310. However, these semiconductor packages are often of a size which decreases or diminishes their utility in certain applications. For example, the semiconductor package 302 is excessively wide due to the outward spacing of the leads 326 from the stacked chips 304 and 310.

An aspect of the present invention overcomes this disadvantage by providing a semiconductor package having a more efficient packaging design. Figure 1 provides a cross-sectional view of a semiconductor package 100 constructed in accordance with an exemplary embodiment of the present invention. The package 100 comprises a plurality of identically configured leads 130 and a die paddle 135. As seen in Figures 1 and 1A, the innermost end of each lead 130 is disposed in spaced relation to the corresponding peripheral edge segment of the die paddle 135. The package 100 further includes a first semiconductor die 110 including a plurality of bond pads 113 which are disposed on the first surface 111a thereof. The package 100 also includes a second semiconductor die 120 which is stacked upon the first semiconductor die 110 and includes a plurality of bond pads 123 disposed on the second surface 121b thereof.

As seen in Figure 1A, the first semiconductor die 110 and leads 130 are arranged relative to each other such that the bond pads 113 of the die 110 are each oriented between a respective pair of leads 130 when the first surface 111a of the first semiconductor die 110 is bonded to the second surfaces 131b of the leads 130, such that none of the bond pads 113 contact any of the second surfaces 131b of the leads 130. Each of the bond pads 113 of the first semiconductor die 110 is connected to the first surface 131a of a respective one of the leads 130 by a first conductive connector 151 such as a conductive wire. Each bond pad 123 of the second semiconductor die 120 is electrically connected to the second surface 131b of a respective one of leads 130 by a second conductive connector 153 such as a conductive wire.

As indicated above, the bond pads 113 of the first semiconductor die 110 are each located between a respective pair of leads 130. Thus, the electrical connection between the bond pads 113 and the first surfaces 131a of the leads 130 through the use of the conductive connectors 151 can be accomplished in a manner wherein the conductive connectors 151 are

each located inwardly relative to the peripheral edge of the first semiconductor die 110 as seen in Figures 1 and 1A. Thus, a more efficiently packaged stacked semiconductor package is provided.

## **VI. ISSUES**

(A). Whether independent Claim 1 and dependent Claims 2-6 and 9 are improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,198,171 to Huang et al. [hereinafter “HUANG”] in view of U.S. Patent No. 6,198,171 to Abe [hereinafter “ABE”]; and whether dependent Claims 7 and 8 are improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over HUANG in view of ABE and Korean Publication No. 2002-0049944 to Song [hereinafter “SONG”].

(B). Whether dependent Claim 11 is improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over HUANG in view of ABE; and

(C). Whether independent Claim 19 and dependent Claims 20-24 are improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over HUANG in view of ABE.

## **VII. GROUPING OF CLAIMS**

For the purpose of this Appeal, Appellant submits that:

- (A). Independent Claim 1 and dependent Claims 2-9 stand or fall together;
- (B). Dependent Claim 11 (from Claim 1) stands alone; and
- (C). Independent Claim 19 and dependent Claims 20-24 stand or fall together.

The reasons why the three groups of claims are believed to be separately patentable are explained below in the following Arguments Section.

## VIII. ARGUMENTS

(A). The rejection of independent Claim 1 and dependent Claims 2-6 and 9 under 35 U.S.C. § 103(a) as being unpatentable over HUANG in view of ABE is in error, the rejection should be reversed, and the application should be remanded to the Examiner with instructions to allow Claims 1-6 and 9. Additionally, the rejection of dependent Claims 7 and 8 under 35 U.S.C. § 103(a) as being unpatentable over HUANG in view of ABE and Korean Publication No. 2002-0049944 to Song [hereinafter “SONG”] is in error, the rejection should be reversed, and the application should be remanded to the Examiner with instructions to allow Claims 7-8.

### The Examiner's Rejection

In regard to independent Claim 1, the Examiner admits that HUANG fails to disclose “portions of the first surface directly attached to the second surface of each of the leads”. The Examiner then submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of HUANG to include portions of the die attached to the leads as disclosed in ABE because it aids in reducing manufacturing costs. Further, the Examiner submits that HUANG and ABE are both from the same field of endeavor, and that the purpose disclosed by ABE would have been recognized in the pertinent art of HUANG.

A Review of HUANG

In the embodiment of the semiconductor package shown in Figure 7 of HUANG, a first or lower chip 304 is shown as being mounted to the top surface of the die pad 318 via a layer of adhesive 322. Disposed about the periphery of the die pad 318 are a plurality of leads 326, each of which includes a first or top surface 328a, and a second or bottom surface 328b which has a stepped structure defining a protruded zone 330. Stacked upon the lower first chip 304 is an upper second chip 310 which is secured to the first chip 304 by a layer of adhesive 324. *As clearly shown in Figure 7, no portion of the lower surface of the chip 304 is attached to the first or top surfaces 328a of the leads 326. Rather, the leads 326 are disposed well outward of the peripheral edges of the first and second chips 304, 310.*

A Review of ABE

ABE discloses a semiconductor device 1 having a leadframe 10 and a semiconductor element 14 which is mounted to the leadframe 10 through the use of an adhesive tape 12. The semiconductor element 14 is electrically connected to the leadframe 10 through the use of bonding wires 16 which, along with the semiconductor element 14, are sealed or encapsulated with a resin material 18. The leadframe 10 of the semiconductor device 1 in the ABE reference includes a plurality of terminal portions 10a which protrude through the substrate mount surface of the resin material 18 and each have a solder layer 19 applied thereto. The application of the solder layer 19 to each of the terminal portions 10a is made possible by the protrusion of the terminal portions 10a through the substrate mount surface of the resin material 18 which allows the terminal portions 10a to be used as connecting terminals, thereby eliminating the need for solder balls for mounting as required in

conventional ball-grid array semiconductor devices, and thus, providing substantially reduced material and manufacturing costs (see ABE specification, column 3, lines 46-58).

*In re Independent Claim 1*

Independent Claim 1 as amended recites, *inter alia*, “. . . portions of the first surface of the first semiconductor die being directly attached to the second surface of each of the leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact the second surface of any one of the leads; . . . ”.

Appellant respectfully submits that the combined teachings of HUANG and ABE clearly do not teach or suggest any embodiment of a semiconductor package having the aforementioned features recited in independent Claim 1.

*Initially, it is noted that the motivation to modify HAUNG with the teachings of ABE as proposed by the Examiner is defective.*

The Examiner contends that it would have been obvious to one of ordinary skill in the art to modify the semiconductor device of HUANG to include portions of the die attached to the leads as disclosed in ABE because it aids in reducing manufacturing cost. Appellant disagrees.

It is well established that it must be shown that there was a suggestion, i.e., a motivation to combine something to suggest the desirability, and thus the obviousness, of making the combination. *Lindermann Maschinenfabrik GMBH v. American Hoist and Derrick Co.*, 730 F.2d 1452, 1462, 221 USPQ 481, 488 (Fed Cir. 1984). Obviousness cannot be established by combining references without also providing evidence of the motivating

force which would impel one skilled in the art to do what the Appellant has done. Ex parte Levengood, 28 USPQ2d 1300, 1302 (Bd Pat. App. & Inter. 1993).

To find motivation, the Examiner makes reference to the passage of the specification of ABE beginning in column 1, line 50 and ending in column 2, line 19. However, this language simply mirrors that described above in column 3, lines 46-58 of the ABE reference. In this regard, both the language of this passage and that cited by the Examiner demonstrates that the reduction in manufacturing costs discussed in ABE has absolutely nothing to do with the attachment of the semiconductor element 14 to the leadframe 10 through the use of the adhesive tape 12. Rather, the manufacturing cost reductions discussed in ABE are achieved by the protrusion of the terminal portions 10a through the substrate mount surface of the resin material 18 and application of the solder layers 19 thereto which allows the terminal portions 10a to be used as connecting terminals. There is simply no teaching or suggestion in the ABE reference regarding a correlation between the reduction in manufacturing costs as argued by the Examiner and the attachment of the semiconductor element 14 to the leadframe 10. Thus, it appears the motivation given by the Examiner to combine the ABE leads to the HUANG package to reduce manufacturing costs is defective.

Accordingly, it is submitted that the Examiner has failed to provide sufficient motivation for the proposed modification, and thus the rejection of at least independent Claim 1 under 35 U.S.C. § 103(a) is improper for the aforementioned reasons and should be withdrawn.

*Additionally, the Appellant's disclosure may not be used as a template for a rejection (i.e. the Examiner has used impermissible hindsight to find motivation).*

Appellant also notes that the Examiner has the initial duty of supplying the factual basis for the rejection and may not, because of doubt that the invention is patentable, resort to speculation, unfounded assumption or hindsight reconstruction to supply deficiencies in the factual basis. See *In re Warner*, 379 F.2d 1011, 1017, 154 USPQ 173, 177 (CCPA 1967). As stated in *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1533, 220 USPQ 303, 312-313 (Fed. Cir. 1983), cert denied, 469 U.S. 851 (1984):

[t]o imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which the inventor taught is used against it teacher.

Appellant submits that it is highly likely that the modification of HUANG in view of ABE as proposed by the Examiner has resulted from a review of Appellant's disclosure and the application of impermissible hindsight to find motivation.

In particular, Appellant submits that the Examiner has merely used the Appellant's disclosure as a template to find obvious the features of independent Claim 1 which recites, *inter alia*, “. . . portions of the first surface of the first semiconductor die being directly attached to the second surface of each of the leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact the second surface of any one of the leads; . . . ”.

Accordingly, it is submitted that the Examiner has used impermissible hindsight to find motivation for the proposed modification, and thus the rejection of at least independent Claim 1 under 35 U.S.C. § 103(a) is improper and should be withdrawn for this additional reason.

**Moreover, the combination which the Examiner presents does not result in the invention that the Appellant claims, therefore, the aforementioned rejection is inappropriate.**

With respect to the aforementioned rejection, the Examiner has not provided a prior art reference or references which teach or suggest **all** the claim limitations of the pending claims.

To establish a prima facie case of obviousness, *the prior art reference (or references when combined) must teach or suggest **all** the claim limitations.* See *Litton Industrial Products, Inc. v. Solid State Systems, Corp.*, 755 F.2d 158, 164, 225 U.S.P.Q. 34, 38 (Fed. Cir. 1985) (“The references fail not only to expressly disclose the claimed invention as a whole, but also to suggest to one of ordinary skill in the art modifications needed to meet **all** the claim limitations”).

Even assuming, *arguendo*, that the hypothetical combination of the HUANG and ABE references is proper (which the Appellant disputes), Appellant respectfully submits that such combination still does not teach or suggest the relative orientations between the bond pads of the first semiconductor die and the leads as recited in independent Claim 1.

As already discussed, a review of Figure 4 of HUANG and the corresponding passage of the specification thereof demonstrates that if the leads 326 were enlarged to extend beneath the first chip 304 or positioned further inboard underneath first chip 304, many if not all of the bonding pads 308 of the first chip 304 would be completely or at least partially covered by the leads 326, as opposed to the bonding pads 308 being oriented between respective pairs of the leads 326.

On the other hand, the present invention clearly teaches and claims a spatial relationship between the bond pads 113 and leads 130. In this regard, there is clearly no

teaching in HUANG regarding the orientation of the first bonding pads 308 of the first chip 304 between respective pairs of the leads 326.

In particular, neither HUANG nor ABE, when considered individually or in combination teach or suggest, *inter alia*, “. . . portions of the first surface of the first semiconductor die being directly attached to the second surface of each of the leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact the second surface of any one of the leads; . . .” as is recited in independent Claim 1.

Accordingly, it is submitted that the proposed combination of HUANG and ABE does not result in the invention recited in at least independent Claim 1, and therefore, the rejection of Claim 1 under 35 U.S.C. § 103(a) is improper for the aforementioned reasons and should be withdrawn.

**And finally, the manner in which the Examiner modifies HUANG in view of ABE renders the HUANG reference unsatisfactory for its intended purpose.**

Appellant submits that the manner in which the Examiner has modified HUANG in view of ABE renders the HUANG reference unsatisfactory for its intended purpose. It is well settled that a proposed modification cannot destroy a reference by rendering the prior art invention being modified unsatisfactory for its intended purpose. *In re Gordon*, 733 F.2d 900, 90, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

As discussed above, the Examiner submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of HUANG to include portions of the die attached to the leads as disclosed in ABE.

A review of Figure 4 of HUANG and the corresponding passage of the specification thereof demonstrates that if the leads 326 were enlarged to extend beneath the first chip 304 or repositioned further inboard beneath first chip 304, many if not all of the bonding pads 308 of the first chip 304 would be completely or at least partially covered by the leads 326, as opposed to the bonding pads 308 being oriented between respective pairs of the leads 326. Therefore, the manner in which the Examiner has modified HUANG in view of ABE renders the HUANG reference unsatisfactory for its intended purpose. Furthermore, neither HUANG or ABE, when considered individually or in combination teach or even remotely suggest the spatial relationship between the bond pads 113 (i.e., the bonding pads 308 being oriented between respective pairs of the leads 326) and leads 130 of the present invention as recited in independent Claim 1.

Accordingly, it is submitted that the Examiner has inappropriately modified HUANG in view of ABE, and as result destroyed the function of the HUANG reference. Thus, Appellant respectfully submits that the rejection of at least independent Claim 1 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

*In re Dependent Claims 2-9*

Furthermore, Appellant submits that dependent Claims 2-9 are allowable at least for the reason that these claims depend from allowable independent Claim 1 and because these claims recite additional features that further define the present invention.

Accordingly, Appellant respectfully submits that the rejection of dependent Claims 2-9 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

**(B). The rejection of dependent Claim 11 under 35 U.S.C. § 103(a) as being unpatentable over HUANG in view of ABE is in error, the rejection should be reversed, and the application should be remanded to the Examiner with instructions to allow dependent Claim 11.**

*The Examiner's Rejection*

In regard to dependent Claim 11, the Examiner submits that HUANG discloses that (a) the first semiconductor die defines a peripheral edge (citing Figure 7); and that (b) the conductive connectors electrically connecting the bond pads of the first semiconductor die to the leads are oriented inwardly relative to the peripheral edge of the first semiconductor die (citing Figure 7).

*In re Dependent Claim 11*

Dependent Claim 11 recites, *inter alia*, “. . . the conductive connectors electrically connecting the bond pads of the first semiconductor die to the leads *are oriented inwardly relative to the peripheral edge of the first semiconductor die*.

Appellant respectfully submits that the combined teachings of HUANG and ABE clearly do not teach or suggest any embodiment of a semiconductor package having the aforementioned features recited in dependent Claim 11.

It is noted that neither HUANG nor ABE teach the conductive connectors (such as wires) electrically connecting the bond pads of a first semiconductor die to the leads being oriented ***inwardly*** relative to the peripheral edge of the first semiconductor die.

For instance, a review of HUANG (all Figures) reveals that wires 216 are oriented *outwardly* relative to the peripheral edge of the semiconductor die 208 – *not inwardly as the*

*Appellant recites in dependent Claim 11.* Furthermore, nowhere in the HUANG reference is there any suggestion that the wires 216 can be or that it is desirable that the HUANG wires be oriented inwardly relative the peripheral edge of the semiconductor die 208.

Also, a review of ABE (all Figures) reveals that wires 16 are oriented outwardly relative to the peripheral edge of the semiconductor die 14 – *not inwardly as the Appellant recites in dependent Claim 11.* Furthermore, nowhere in the ABE reference is there any suggestion that the ABE wires 16 can be or that it is desirable that the ABE wires 16 be oriented inwardly relative the peripheral edge of semiconductor die 14. If anything, ABE teaches away from the aforementioned feature recited in dependent Claim 11. For instance, it is noted that ABE does not even teach a die pad to which the ABE die 14 may be attached. Instead, ABE utilizes adhesive tape 12 to attach the die 14 to the top portion of the lead frame 10. Therefore, it is apparent that the ABE adhesive tape 12 would not allow the ABE wires to be routed inward.

Accordingly, Appellant respectfully submits that the rejection of dependent Claim 11 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

**(C). The rejection of independent Claim 19 and dependent Claims 20-24 under 35 U.S.C. § 103(a) as being unpatentable over HUANG in view of ABE is in error, the rejection should be reversed, and the application should be remanded to the Examiner with instructions to allow Claims 19-24.**

*The Examiner's Rejection*

In regard to independent Claim 19, the Examiner admits that HUANG fails to disclose “portions of the first surface directly attached to the second surface of each of the

leads”. The Examiner then submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of HUANG to include portions of the die attached to the leads as disclosed in ABE because it aids in reducing manufacturing costs. Further, the Examiner submits that HUANG and ABE are both from the same field of endeavor, and that the purpose disclosed by ABE would have been recognized in the pertinent art of HUANG.

*In re Claims Independent Claim 19*

Independent Claim 19 as amended recites, *inter alia*, “. . . the first semiconductor die being directly attached to each of the leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact any of the leads; . . . ”.

Appellant respectfully submits that the combined teachings of HUANG and ABE clearly do not teach or suggest any embodiment of a semiconductor package having the aforementioned features recited in independent Claim 19.

*Once again, it is noted that the motivation to modify HUANG with the teachings of ABE as proposed by the Examiner is defective.*

The Examiner contends that it would have been obvious to one of ordinary skill in the art to modify the semiconductor device of HUANG to include portions of the die attached to the leads as disclosed in ABE because it aids in reducing manufacturing cost. Appellant disagrees.

To find motivation, the Examiner makes reference to the passage of the specification of ABE beginning in column 1, line 50 and ending in column 2, line 19. However, this

language simply mirrors that described above in column 3, lines 46-58 of the ABE reference. In this regard, both the language of this passage and that cited by the Examiner demonstrates that the reduction in manufacturing costs discussed in ABE has absolutely nothing to do with the attachment of the semiconductor element 14 to the leadframe 10 through the use of the adhesive tape 12. Rather, the manufacturing cost reductions discussed in ABE are achieved by the protrusion of the terminal portions 10a through the substrate mount surface of the resin material 18 and application of the solder layers 19 thereto which allows the terminal portions 10a to be used as connecting terminals. There is simply no teaching or suggestion in the ABE reference regarding a correlation between the reduction in manufacturing costs as argued by the Examiner and the attachment of the semiconductor element 14 to the leadframe 10. Thus, it appears the motivation given by the Examiner to combine the ABE leads to the HUANG package to reduce manufacturing costs is defective.

Accordingly, it is submitted that the Examiner has failed to provide sufficient motivation for the proposed modification, and thus the rejection of at least independent Claim 19 under 35 U.S.C. § 103(a) is improper for the aforementioned reasons and should be withdrawn.

**Additionally, the Appellant's disclosure may not be used as a template for a rejection (i.e. the Examiner has used impermissible hindsight to find motivation).**

Appellant submits that it is highly likely that the modification of HUANG in view of ABE as proposed by the Examiner has resulted from a review of Appellant's disclosure and the application of impermissible hindsight to find motivation.

In particular, Appellant submits that the Examiner has merely used the Appellant's disclosure as a template to find obvious the features of independent Claim 19 as amended

which recites, *inter alia*, “. . . the first semiconductor die being directly attached to each of the leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact any of the leads; . . . ”.

Accordingly, it is submitted that the Examiner has used impermissible hindsight to find motivation for the proposed modification, and thus the rejection of at least independent Claim 19 under 35 U.S.C. § 103(a) is improper and should be withdrawn for this additional reason.

**Moreover, the combination which the Examiner presents does not result in the invention that the Appellant claims, therefore, the aforementioned rejection is inappropriate.**

With respect to the aforementioned rejection, the Examiner has not provided a prior art reference or references which teach or suggest **all** the claim limitations of the pending claims.

Even assuming, *arguendo*, that the hypothetical combination of the HUANG and ABE references is proper (which the Appellant disputes), Appellant respectfully submits that such combination still does not teach or suggest the relative orientations between the bond pads of the first semiconductor die and the leads as recited in independent Claim 19.

As already discussed, a review of Figure 4 of HUANG and the corresponding passage of the specification thereof demonstrates that if the leads 326 were enlarged to extend beneath the first chip 304 or positioned further inboard underneath first chip 304, many if not all of the bonding pads 308 of the first chip 304 would be completely or at least partially covered by the leads 326, as opposed to the bonding pads 308 being oriented between respective pairs of the leads 326.

On the other hand, the present invention clearly teaches and claims a spatial relationship between the bond pads 113 and leads 130. In this regard, there is clearly no teaching in HUANG regarding the orientation of the first bonding pads 308 of the first chip 304 between respective pairs of the leads 326.

In particular, neither HUANG nor ABE, when considered individually or in combination teach or suggest, *inter alia*, “. . . the first semiconductor die being directly attached to each of the leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact any of the leads; . . . ” as is recited in independent Claim 19.

Accordingly, it is submitted that the proposed combination of HUANG and ABE does not result in the invention recited in at least independent Claim 19, and therefore, the rejection of Claim 19 under 35 U.S.C. § 103(a) is improper for the aforementioned reasons and should be withdrawn.

**And finally, the manner in which the Examiner modifies HUANG in view of ABE renders the HUANG reference unsatisfactory for its intended purpose.**

Appellant submits that the manner in which the Examiner has modified HUANG in view of ABE renders the HUANG reference unsatisfactory for its intended purpose.

As discussed above, the Examiner submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of HUANG to include portions of the die attached to the leads as disclosed in ABE.

A review of Figure 4 of HUANG and the corresponding passage of the specification thereof demonstrates that if the leads 326 were enlarged to extend beneath the first chip 304

or repositioned further inboard beneath first chip 304, many if not all of the bonding pads 308 of the first chip 304 would be completely or at least partially covered by the leads 326, as opposed to the bonding pads 308 being oriented between respective pairs of the leads 326. Therefore, the manner in which the Examiner has modified HUANG in view of ABE renders the HUANG reference unsatisfactory for its intended purpose. Furthermore, neither HUANG or ABE, when considered individually or in combination teach or even remotely suggest the spatial relationship between the bond pads 113 (i.e., the bonding pads 308 being oriented between respective pairs of the leads 326) and leads 130 of the present invention as recited in independent Claim 19.

Accordingly, it is submitted that the Examiner has inappropriately modified HUANG in view of ABE, and as result destroyed the function of the HUANG reference. Thus, Appellant respectfully submits that the rejection of at least independent Claim 19 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

*In re Dependent Claims 20-24*

Furthermore, Appellant submits that dependent Claims 20-24 are allowable at least for the reason that these claims depend from allowable independent Claim 19 and because these claims recite additional features that further define the present invention.

Accordingly, Appellant respectfully submits that the rejection of dependent Claims 20-24 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

***Application is Allowable***

Appellant respectfully submits that each and every pending claim of the present application meets the requirements for patentability, and respectfully requests that the Board remand the present application to the Examiner instructing the Examiner to allow the present application.

**CONCLUSION**

In view of the foregoing, it is submitted that none of the references of record, when considered either alone or in any proper combination thereof, anticipate or render obvious the Appellant's invention as recited in Claims 1-9, 11 and 19-24. The applied references of record have been discussed and distinguished, while significant claimed features of the present invention have been pointed out.

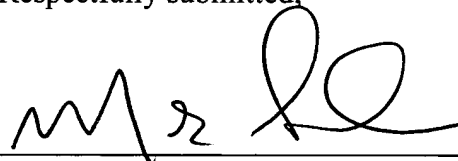
Appellant respectfully submits that each and every pending claim of the present invention meets the requirements for patentability under 35 U.S.C. §§ 112, 102 and 103, and requests that all of the aforementioned rejections be reversed by the Board, and the application be remanded to the Examiner for withdrawal of all the rejections and allowance of all pending claims.

Accordingly, immediate allowance of the claims in the present application is respectfully requested and believed to be appropriate.

Respectfully submitted,

Date: 10/12/04

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## APPENDIX

### CLAIMS ON APPEAL

1. (Previously Presented) A semiconductor package comprising:
  - a plurality of leads, each of the leads defining:
    - a first surface;
    - a second surface disposed in opposed relation to the first surface; and
    - a third surface disposed in opposed relation to the second surface, the first surface being oriented between the second and third surfaces;
  - a first semiconductor die defining opposed first and second surfaces and including a plurality of bond pads disposed on the first surface thereof, portions of the first surface of the first semiconductor die being directly attached to the second surface of each of the leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact the second surface of any one of the leads;
  - a second semiconductor die defining opposed first and second surfaces and including a plurality of bond pads disposed on the second surface thereof, the first surface of the second semiconductor die being attached to the second surface of the first semiconductor die;
  - a plurality of conductive connectors electrically connecting the bond pads of the first and second semiconductor dies to respective ones of the leads; and
  - an encapsulating portion applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the conductive connectors.
2. (Original) The semiconductor package of Claim 1 wherein the conductive connectors comprise conductive wires.
3. (Previously Presented) The semiconductor package of Claim 1 wherein:
  - the conductive connectors comprise first and second conductive wires;
  - the bond pads of the first semiconductor die are electrically connected to respective ones of the first surfaces of the leads by the first conductive wires; and

the bond pads of the second semiconductor die are electrically connected to respective ones of the second surfaces of the leads by the second conductive wires.

4. (Original) The semiconductor package of Claim 1 further comprising:

a die paddle defining opposed top and bottom surfaces, the leads being disposed about the die paddle;

the first surface of the first semiconductor die further being attached to the top surface of the die paddle.

5. (Original) The semiconductor package of Claim 4 wherein:

the first surface of the first semiconductor die is attached to the second surface of each of the leads and to the top surface of the die paddle by a first bonding means; and

the first surface of the second semiconductor die is attached to the second surface of the first semiconductor die by a second bonding means.

6. (Original) The semiconductor package of Claim 4 wherein:

the die paddle is formed to have a die paddle thickness;

each of the leads is formed to have a lead thickness between the second and third surfaces thereof; and

the die paddle thickness is substantially equal to the lead thickness.

7. (Original) The semiconductor package of Claim 4 wherein the encapsulating portion is applied to the die paddle such that the bottom surface of the die paddle is exposed within the encapsulating portion.

8. (Original) The semiconductor package of Claim 7 wherein the encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

9. (Original) The semiconductor package of Claim 1 wherein the encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

10. (Cancelled)

11. (Previously Presented) The semiconductor package of Claim 1 wherein:

the first semiconductor die defines a peripheral edge; and

the conductive connectors electrically connecting the bond pads of the first semiconductor die to the leads are oriented inwardly relative to the peripheral edge of the first semiconductor die.

12-18. (Cancelled)

19. (Previously Presented) A semiconductor package comprising:

a plurality of leads;

a first semiconductor die including a plurality of bond pads disposed thereon, the first semiconductor die being directly attached to each of the leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact any of the leads;

a second semiconductor die including a plurality of bond pads disposed thereon, the second semiconductor die being attached to the first semiconductor die;

means for electrically connecting the bond pads of the first and second semiconductor dies to respective ones of the leads; and

an encapsulating portion applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the electrical connection means.

20. (Previously Presented) The semiconductor package of Claim 19 wherein the electrical connection means comprises conductive wires.

21. (Previously Presented) The semiconductor package of Claim 20 wherein:

each of the leads defines opposed first and second surfaces and a third surface which is opposed to the second surface, the first surface being oriented between the second and third surfaces;

the bond pads of the first semiconductor die are electrically connected to respective ones of the first surfaces of the leads by first conductive wires; and

the bond pads of the second semiconductor die are electrically connected to respective ones of the second surfaces of the leads by second conductive wires.

22. (Previously Presented) The semiconductor package of Claim 21 wherein the encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

23. (Previously Presented) The semiconductor package of Claim 19 further comprising:

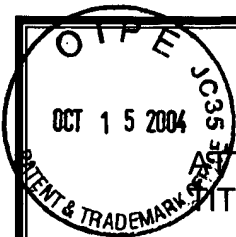
a die paddle, the leads being disposed about the die paddle;  
the first semiconductor die being attached to the die paddle.

24. (Previously Presented) The semiconductor package of Claim 23 wherein:

the die paddle defines opposed top and bottom surfaces, with the first semiconductor die being attached to the top surface of the die paddle; and

the encapsulating portion is applied to the die paddle such that the bottom surface of the die paddle is exposed within the encapsulating portion.

25. (Cancelled)



ATTORNEY DOCKET NO: AMKOR-017RCE  
TITLE: SEMICONDUCTOR PACKAGE WITH STACKED DIES

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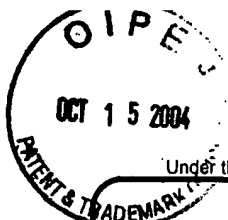
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<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Application Number	10/043,946
	Filing Date	01/11/2002
	First Named Inventor	Jong Sik Paek
	Art Unit	6383
	Examiner Name	Lewis, Monica
Total Number of Pages in This Submission	Attorney Docket Number	AMKOR-017RCE

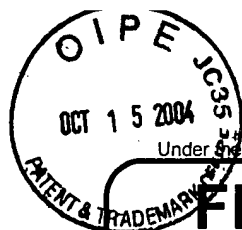
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# FEE TRANSMITTAL for FY 2005

Effective 10/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$) 340

## Complete if Known

Application Number 10/043,946  
Filing Date 01/11/2002  
First Named Inventor Jong Sik Paek  
Examiner Name Monica Lewis  
Art Unit 6383  
Attorney Docket No. AMKOR-017RCE

## METHOD OF PAYMENT (check all that apply)

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## FEE CALCULATION

### 1. BASIC FILING FEE

Large Entity Fee Code	Small Entity Fee Code	Fee (\$)	Fee (\$)	Fee Description	Fee Paid
1001	2001	790	395	Utility filing fee	
1002	2002	350	175	Design filing fee	
1003	2003	550	275	Plant filing fee	
1004	2004	790	395	Reissue filing fee	
1005	2005	160	80	Provisional filing fee	
SUBTOTAL (1)					0

### 2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Total Claims	Extra Claims	Fee from below	Fee Paid
Independent	-20** =	X	
Multiple Dependent	-3** =	X	

<u>Large Entity</u>		<u>Small Entity</u>		<u>Fee Description</u>
Fee Code	Fee (\$)	Fee Code	Fee (\$)	
1202	18	2202	9	Claims in excess of 20
1201	88	2201	44	Independent claims in excess of 3
1203	300	2203	150	Multiple dependent claim, if not paid
1204	88	2204	44	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

\*\*or number previously paid, if greater; For Reissues, see above

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

Large Entity Fee Code	Small Entity Fee Code	Fee (\$)	Fee (\$)	Fee Description	Fee Paid
1051	2051	130	65	Surcharge - late filing fee or oath	
1052	2052	50	25	Surcharge - late provisional filing fee or cover sheet	
1053	1053	130	130	Non-English specification	
1812	1812	2,520	2,520	For filing a request for ex parte reexamination	
1804	1804	920*	920*	Requesting publication of SIR prior to Examiner action	
1805	1805	1,840*	1,840*	Requesting publication of SIR after Examiner action	
1251	2251	110	55	Extension for reply within first month	
1252	2252	430	215	Extension for reply within second month	
1253	2253	980	490	Extension for reply within third month	
1254	2254	1,530	765	Extension for reply within fourth month	
1255	2255	2,080	1,040	Extension for reply within fifth month	
1401	2401	340	170	Notice of Appeal	
1402	2402	340	170	Filing a brief in support of an appeal	340
1403	2403	300	150	Request for oral hearing	
1451	2451	1,510	1,510	Petition to institute a public use proceeding	
1452	2452	110	55	Petition to revive - unavoidable	
1453	2453	1,370	685	Petition to revive - unintentional	
1501	2501	1,370	685	Utility issue fee (or reissue)	
1502	2502	490	245	Design issue fee	
1503	2503	660	330	Plant issue fee	
1460	1460	130	130	Petitions to the Commissioner	
1807	1807	50	50	Processing fee under 37 CFR 1.17(q)	
1806	1806	180	180	Submission of Information Disclosure Stmt	
8021	8021	40	40	Recording each patent assignment per property (times number of properties)	
1809	2809	790	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	2810	790	395	For each additional invention to be examined (37 CFR 1.129(b))	
1801	2801	790	395	Request for Continued Examination (RCE)	
1802	1802	900	900	Request for expedited examination of a design application	
Other fee (specify)					
*Reduced by Basic Filing Fee Paid					
SUBTOTAL (3)					340

## SUBMITTED BY

(Complete if applicable)

Name (Print/Type) Mark B. Garred Registration No. 34,823 Telephone (949) 855-1246  
Signature [Signature] (Attorney/Agent) Date October 12, 2004

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